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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

# Office Action Summary

## Application No.

10/561,270

## Applicant(s)

FURIHATA ET AL.

## Examiner

VINH T. LAM

## Art Unit

2629

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 01 May 2009.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) 13-17 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-12 and 18-20 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 19 December 2005 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☒ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/S508)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_

## DETAILED ACTION

### *Claim Rejections - 35 USC § 112*

The following is a quotation of the **first paragraph** of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

1. Claims **1** and **18** are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Regarding Claim **1**, the specification as originally filed has failed to provide support for the recitation of "... wherein **transfer** of said **first bitmap** data **from** said **graphic engine** to said **work memory**, **transfer** of said **second bitmap** data **from** said **work memory** to **display memory**, and **transfer** of said **second bitmap** data **from** said **display memory** to said **driver circuit** are allowed to be performed at the **same time** ...". The specification does not reasonably convey one skill in the art how to make or use applicant claimed invention for "... wherein **transfer** of said **first bitmap** data **from** said **graphic engine** to said **work memory**, **transfer** of said **second bitmap** data **from** said **work memory** to **display memory**, and **transfer** of said **second bitmap** data **from** said **display memory** to said **driver circuit** are allowed to be performed at the **same time** ...".

Regarding Claim **18**, the specification as originally filed has failed to provide support for the recitation of

"... wherein said **first bitmap data** corresponds **only to a portion** of an image and that **cannot be directly used to display** the image on said display panel,

wherein said **second bit data** corresponding to an **entirety** of the image and that can be directly **used to display** the image on said display panel ..."

. The specification does not reasonably convey one skill in the art how to make or use applicant claimed invention for

"... wherein said **first bitmap data** corresponds **only to a portion** of an image and that **cannot be directly used to display** the image on said display panel,

wherein said **second bit data** corresponding to an **entirety** of the image and that can be directly **used to display** the image on said display panel ...".

The following is a quotation of the **second paragraph** of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims **1** and **18** is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The limitation of Claim **1** "... wherein **transfer** of said **first bitmap data** from said **graphic engine** to said **work memory**, **transfer** of said **second bitmap data** from said **work memory** to **display memory**, and **transfer** of said **second bitmap**

data **from** said **display memory** to said **driver circuit** are allowed to be performed at the **same time ...**" is not clear.

First of all, since said **second bitmap** data is developed from said **first bitmap** data, said **first bitmap** data are totally and entirely transformed into said **second bitmap** data? That is there are no **first bitmap** data after Work Memory 12?

Secondly, what are the differences between said **second bitmap data from said work memory** and said **second bitmap data from said display memory**? Or are they the same? If so, what is the purpose of Display Memory 13?

Finally, if the said **second bitmap data** are developed from said **first bitmap** data, how are said **first bitmap data** and said **second bitmap data** performed at the **same time**?

To further advance prosecution, the Examiner interprets that:

**transfer** of said **first bitmap** (i.e. a random bitmap (i)) data **from** said **graphic engine** to said **work memory**,

**transfer** of said **second bitmap** (i.e. another bitmap (j)) data **from** said **work memory** to **display memory**,

and **transfer** of said **second bitmap** (i.e. yet another bitmap (k) different from both i and j bitmaps, wherein i, j, and k are not necessarily consecutive bitmaps processed in time) data **from** said **display memory** to said **driver circuit** are allowed to be performed at the **same time** (i.e. the same number of data **bits** or data **lines** of said **first bitmap** are transferred at the same time; Specification [0013] and [0014]).

The limitation of Claim 18

"... wherein said **first bitmap data** corresponds **only to a portion** of an image and that **cannot be directly used to display** the image on said display panel,

wherein said **second bit data** corresponding to an **entirety** of the image and that can be directly **used to display** the image on said display panel ..." is not clear.

First of all concerning said **first bitmap data**, why is **only to a portion** of an image and that **cannot be directly used to display** the image? Which **portion of first bitmap data** that **cannot be directly used to display**? Can the **other portions** be **directly used to display** the image? If so, what are the differences between a **portion** of an image that **cannot be directly used to display** and the **other portions** that can be **directly used to display** the image? What is **directly used to display** the image meant?

Secondly concerning said **second bitmap data**, why the **entirety** of the image and that can be directly **used to display** the image? As discussed above, there are two **second bitmap data**, namely one are outputted from the Work Memory and the other are outputted from the Display Memory, which of said **second bit data** corresponding to an **entirety** of the image and that can be directly **used to display** the image?

Thirdly, Specification in contrary discloses that either the **first bitmap data** or the **second bitmap data** can be used to display the image ([0021]).

Finally, bitmap data from the work memory 12 to the display memory 13 (i.e. **second bitmap data**) are incomplete image, that is, a portion of the image to be displayed ([0075]).

To further advance prosecution, the Examiner interprets that some of either the **first bitmap data** or the **second bitmap data** can be used to display the image.

These limitations also, therefore, invoke 35 USC 112 1<sup>st</sup> ¶ as rejected above.

3. Claim 4 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The limitation of Claim 4 "... and **bitmap data** directly from said work memory ..." is not clear.

Which (or what are transferred) **bitmap data** directly from said work memory?

Are **bitmap data** referred to said first or second bitmap data?

This limitation seems to repeat from the immediately precedent limitation of Claim 4.

To further advance prosecution, the Examiner disregards the above limitation.

Appropriate correction is required.

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) a patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 1-5 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Chadha (US Pub. No. 2003/0184552)** in view of **Adachi (US Patent No. US 5636336)**.

Regarding Claim 1, (Currently Amended) **Chadha** teaches a controller/driver comprising:

a work memory ([0037], FIG. 6);

a graphic engine converting externally received image data into first bitmap data, and storing said bitmap data into said work memory ([0037], FIG. 6);

a display memory receiving and storing second bitmap data developed from said first bitmap data stored in said work memory ([0037], FIG. 6); and

a driver circuit (inherently driving C columns and R rows) which receives said second bitmap data from said display memory, and drives a display panel in response to said second bitmap data received from said display memory ([0040], FIG. 6);

wherein transfer of said first bitmap data from said graphic engine to said work memory, transfer of said second bitmap data from said work memory to display memory, and transfer of said second bitmap data from said display memory to said driver circuit are allowed to be performed at the same time (i.e. Graphics Engine 1 (GE1) 606 generates the image display data and outputs this image display data to the processed image buffer of PIM 602; [0038], FIG. 6).

However, **Chadha** does not teach connections among the graphic engine, work memory, display memory, and driver circuit.

In the same field of endeavor, **Adachi** teaches:



wherein said work memory (i.e. **48** of graphic data processing means **22**; FIG. **3**) has first (i.e. connection between graphic data processing means **22** and instruction detection section **34**; Col. **6**, Ln. **34-39**, FIG. **3**) and second (i.e. connection between graphic data processing means **22** and display **24**; Col. **6**, Ln. **22-24**, FIG. **3**) separate ports, said first port being connected to said graphic engine (Col. **7**, Ln. **17-20**, FIG. **3**), wherein said display memory (i.e. **60**; Col. **7**, Ln. **17-20**, FIG. **3**) has third and fourth separate ports, said third port being connected to said second port, and said fourth port being connected to said driver circuit (i.e. display screen **62** obviously includes driver circuit; Col. **7**, Ln. **17-20**, FIG. **3**).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to combine **Chadha** teaching of a work memory, a graphic engine, a display memory, and a driver circuit with **Adachi** teaching of connections among the graphic engine, work memory, display memory, and driver circuit in order to benefit of reducing power consumption and latency by having a controller/driver comprising of the graphic engine, work memory, display memory, driver circuit, and of connections among the graphic engine, work memory, display memory, and driver circuit.

Regarding Claim **2**, (Original) the controller/driver according to claim **1**, wherein **Chadha** teaches said image data is described in a vector format (e.g. XML image file; Col. **2**, [0033], FIG. **3**).

Regarding Claim 3, (Original) the controller/driver according to claim 1, wherein **Chadha** teaches said image data includes compressed image data (e.g. GIF image file; Col. 2, [0033], FIG. 3).

Regarding Claim 4, (Currently Amended) **Chadha** and **Adachi** teach the controller/driver according to claim 1, wherein **Chadha** teaches

said second bitmap data is developed on said display memory through data transfer of said first bitmap data directly from said work memory, and bitmap data directly from said work memory (i.e. Processed Image Memory 602 from Raw Data Memory 600; [0038], FIG. 6); and

said data transfer of said first bitmap data from said work memory to said display memory is performed such that a set of data bits of said first bitmap data are transferred at the same time (i.e. Graphics Engine 1 (GE1) 606 generates the image display data and outputs this image display data to the processed image buffer of PIM 602; [0038], FIG. 6).

Regarding Claim 5, (Original) the controller/driver according to claim 4, wherein **Chadha** teaches said first bitmap data includes a plurality of line data each associated with a line of pixels of an image represented by said second bitmap data to be displayed ([0040], FIG. 6), and

wherein said data transfer of said first bitmap data from said work memory to said display memory is performed such that each of said line data is transferred at the same time (i.e. Graphics Engine 1 (GE1) 606 generates the image display data and

outputs this image display data to the processed image buffer of PIM 602; [0038], FIG.

6).

Regarding Claim 18, (New) the controller/driver according to claim 1,

**Chadha** teaches

wherein said controller/driver controls and drives a display panel ([0036], FIG. 5),

wherein said first bitmap data corresponds only to a portion of an image and that cannot be directly used to display the image on said display panel ([0038], FIG. 5),

wherein said second bit data corresponding to an entirety of the image and that can be directly used to display the image on said display panel ([0039], FIG. 5), and

wherein said display memory is directly connected to said work memory ([0040], FIG. 5).

6. Claims 6-12, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Chadha (US Patent Application Publication No. 2003/0184552)** in view of **Adachi (US Patent No. US 5636336)** and further in view of **Yamazaki et al. (US Patent No. 5726947)**.

Regarding Claim 6, (Currently Amended) **Chadha** and **Adachi** teach the controller/driver according to claim 5.

However, **Chadha** and **Adachi** do not teach a latch receiving said line data from said work memory and display memory receiving said line data from said latch.

In the same field of endeavor, **Yamazaki et al.** further teach:

a latch receiving said line data from said work memory, and temporally storing said received line data (Col. 2, Ln. 43-45, FIG. 25),

wherein said display memory receives said line data from said latch (Col. 2, Ln. 42-53, FIG. 25).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to combine **Chadha** and **Adachi** teachings of first bitmap data including a plurality of line data and data transfer of said first bitmap data from said work memory to said display memory performing such that each of said line data transferring at the same time with **Yamazaki et al.** teaching of a latch receiving said line data from said work memory and display memory receives said line data from said latch in order to benefit of reducing power consumption and latency by having first bitmap data including a plurality of line data, data transfer of said first bitmap data from said work memory to said display memory performing such that each of said line data transferring at the same time, a latch receiving said line data from said work memory, and display memory receiving said line data from said latch.

Regarding Claim 7, (Original) **Chadha** and **Adachi** teach the controller/driver according to claim 5.

However, **Chadha** and **Adachi** do not teach a controller controlling said work memory, said display memory, and said driver circuit so that said data transfer of said first bitmap data from said work memory to said display memory is synchronous with readout of said second bitmap data from said display memory to said driver circuit.

In the same field of endeavor, **Yamazaki et al.** further teach:

a controller controlling said work memory, said display memory, and said driver circuit so that said data transfer of said first bitmap data from said work memory to said display memory is synchronous with readout of said second bitmap data from said display memory to said driver circuit (Col. 1, Ln. **24-41**, FIG. **22**).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to combine **Chadha** and **Adachi** teachings of first bitmap data including a plurality of line data and data transfer of said first bitmap data from said work memory to said display memory performing such that each of said line data transferring at the same time with **Yamazaki et al.** teaching of a controller controlling said work memory, said display memory, and said driver circuit so that said data transfer of said first bitmap data from said work memory to said display memory is synchronous with readout of said second bitmap data from said display memory to said driver circuit in order to benefit of reducing power consumption and latency by having first bitmap data including a plurality of line data and data transfer of said first bitmap data from said work memory to said display memory performing such that each of said line data transferring at the same time, wherein a controller controlling said work memory, said display memory, and said driver circuit so that said data transfer of said first bitmap data from said work memory to said display memory is synchronous with readout of said second bitmap data from said display memory to said driver circuit.

Regarding Claim **8**, (Original) the controller/driver according to claim 7, wherein **Chadha** teaches said data transfer of said first bitmap data from said work

memory to said display memory is initiated in response to activation of a frame synchronization signal indicating to start displaying each image frame ([0076], FIG. 13).

Regarding Claim 9, (Original) the controller/driver according to claim 7, wherein **Yamazaki et al.** teach said controller controls said display memory, and said driver circuit so that said data transfer of said first bitmap data from said work memory to said display memory does not overrun said readout of said second bitmap data from said display memory to said driver circuit (Col. 3, Ln. 27-47, FIG. 26).

Regarding Claim 10, (Original) **Chadha** and **Adachi** teach the controller/driver according to claim 1.

However, **Chadha** and **Adachi** do not teach the internal structures of work and display memories and connections between them.

In the same field of endeavor, **Yamazaki et al.** further teach wherein said work memory includes:

a plurality of first bit lines , a plurality of first word lines (Col. 7, Ln. 4-5, FIG. 1),  
and

a plurality of first memory cells disposed at respective intersections of said first bit lines and first word lines to store therein said first bitmap data (Col. 7, Ln. 5-6),

wherein said display memory includes:

a plurality of second bit lines, a plurality of second word lines (Col. 7, Ln. 7-9, FIG. 1), and

a plurality of second memory cells disposed at respective intersections of said second bit lines and second word lines to store therein said second bitmap data (Col. 7, Ln. 9-10, FIG. 1),

wherein a number of said first bit lines is same as that of said second bit lines (Col. 7, Ln. 4-8, FIG. 1),, and

wherein said first bit lines are connected to said second bit lines, respectively (Col. 7, Ln. 12-20, FIG. 1).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to combine **Chadha** and **Adachi** teachings of a controller/driver comprising of the graphic engine, work memory, display memory, driver circuit, and of connections among the graphic engine, work memory, display memory, and driver circuit with **Yamazaki et al.** teaching of the internal structures of the work and display memories in order to benefit of reducing power consumption and latency by having a controller/driver comprising of the graphic engine, work memory, display memory, driver circuit, of connections among the graphic engine, work memory, display memory, and driver circuit, and the internal structures of the work and display memories.

Regarding Claim 11, (Original) the controller/driver according to claim 10, wherein **Yamazaki et al.** teach a number of said first word lines is identical to that of said second word lines (Col. 7, Ln. 4-8, FIG. 1).

Regarding Claim 12, (Currently Amended) the controller/driver according to claim 10, **Yamazaki et al.** further teach

a timing controller controlling said work memory, and said display memory, and said driver circuit (Col. 1, Ln. 23-40, FIG. 26),

wherein said driver circuit is connected to said second bit lines (i.e. bus RAM 32a or 32; Col. 3, Ln. 39-41, FIGs. 25 & 26), and wherein said timing controller is adapted to deactivate said display memory to allow said first bitmap data to be transmitted from said work memory to said driver circuit through said second bit lines (Col. 3, Ln. 39-44, FIG. 26).

Regarding Claim 19, (New) the controller/driver according to claim 1, **Yamazaki et al.** further teach:

a latch receiving said first bitmap data from said work memory, and temporally storing said first bitmap data (Col. 2, Ln. 43-53, FIG. 25); and

a timing controller for controlling output of data from said latch, wherein said display memory receives said first bitmap data output from said latch (Col. 23, Ln. 31-41, FIG. 17),

wherein said work memory and said display memory are operated at different times due to having said latch provided therebetween (Col. 23, Ln. 31-41, FIG. 17).

7. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Chadha (US Patent Application Publication No. 2003/0184552)** in view of **Adachi (US Patent No. US 5636336)** and further in view of **Patrick et al. (US Patent No. 5644758)**.

Regarding Claim 20, (New) the controller/driver according to claim 1, **Chadha** further teaches:



means for transferring said first bitmap data from said work memory to said display memory ([0037], FIG. 6); and

means for displaying said second bitmap data output from said display memory on said display panel ([0037], FIG. 6).

However, **Chadha and Adachi** do not teach a first rate at which said first bitmap data is transferred from said work memory to said display memory is faster than a second rate at which said second bitmap data is output from said display memory for display on said display panel.

In the same field of endeavor, **Patrick et al.** further teach a first rate at which said first bitmap data is transferred from said work memory to said display memory is faster than a second rate at which said second bitmap data is output from said display memory for display on said display panel (Col. 2, Ln. 1-10).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to combine **Chadha and Adachi** teachings of a controller/driver comprising of the graphic engine, work memory, display memory, driver circuit, and of connections among the graphic engine, work memory, display memory, and driver circuit with **Patrick et al.** teaching of a first rate at which said first bitmap data is transferred from said work memory to said display memory is faster than a second rate at which said second bitmap data is output from said display memory for display on said display panel in order to benefit of reducing the power consumption and latency by having a controller/driver comprising of the graphic engine, work memory, display memory, driver circuit, and of connections among the graphic engine, work memory,

display memory, driver circuit, wherein a first rate at which said first bitmap data is transferred from said work memory to said display memory is faster than a second rate at which said second bitmap data is output from said display memory for display on said display panel.

***Response to Arguments/Amendment/Remarks***

8. Applicant's arguments with respect to claims 1-12 have been considered but are moot in view of the new ground(s) of rejection.
9. Regarding Claims **13-17** are withdrawn.

***Conclusion***

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to VINH T. LAM whose telephone number is (571)270-3704. The examiner can normally be reached on M-F (7:00-4:30) EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amare Mengistu can be reached on (571) 272-7674. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/VTL/

/Amare Mengistu/  
Supervisory Patent Examiner, Art Unit 2629